In the Specification:

Please replace the paragraph beginning on page 8, line 7, with the following rewritten paragraph:

According to yet another aspect of the semiconductor integrated circuit of the present invention, the first current source and the second current source have a ~~second~~third transistor and a ~~third~~fourth transistor respectively whose gates are connected to the first node. The ~~second~~third and the ~~third~~fourth transistors constitute a ~~first~~second current mirror circuit. This makes it possible to make the power supply current generated in the second current source equal to the current generated in the first current source. As a result, the power supply current supplied to the internal circuit is accurately adjusted under correction control by the correcting circuit.

Please replace the paragraph beginning on page 14, line 3, with the following rewritten paragraph:

The voltage generating unit VGEN has a pMOS transistor PM11 (first current source, ~~second~~third transistor), an nMOS transistor NM11, and a resistor R1 (load circuit) that are connected in series between a power supply line VDD and a ground line VSS. A gate of the pMOS transistor PM11 is connected to a drain (first node ND1). A gate of the nMOS transistor NM11 receives the constant voltage V1. A connecting node ND3 between the nMOS transistor NM11 and the resistor R1 is connected to one input of the amplifier AMP. The voltage of the connecting node ND3 is independent of the temperature variation

and the variation of the threshold voltage, and is kept at 1.2 V based on the feedback from the connecting node ND3 to the amplifier AMP. Consequently, a predetermined voltage (first voltage) is generated at the first node ND1.

Please replace the paragraph beginning on page 14, line 13, with the following rewritten paragraph:

The constant-current source 12 has a plurality of pMOS transistors PM2 (PM21, PM22, ...; second current source, ~~third~~fourth transistor). The pMOS transistors PM2 are connected to power supply lines VDD at sources thereof, and connected to the node ND1 at gates thereof. Drains of the pMOS transistors PM2 are connected to the internal circuits 16a, 16b, ..., respectively.

Please replace the paragraph beginning on page 14, line 18, with the following rewritten paragraph:

The pMOS transistors PM2 of the constant-current source 12 and the pMOS transistor PM11 of the bias circuit 10 constitute current mirror circuits (~~first~~second current mirror circuit) respectively. Consequently, a drain-to-source current I1 (first current) of the pMOS transistor PM11 becomes equal to each of source-to-drain currents I2 (I21, I22, ...; power supply current) of the pMOS transistors PM2. Therefore, each of the currents I21, I22, ... supplied to the internal circuits 16a, 16b, ..., becomes equal to the current I1 flowing through the bias circuit 10.

Please replace the paragraph beginning on page 14, line 25, with the following rewritten paragraph:

The correcting circuit 14 has pMOS transistors PM31, PM32 (~~fourth~~second transistor) that constitute a current mirror circuit (~~second~~first current mirror circuit) and an nMOS transistor NM31 (correcting transistor). Sources of the pMOS transistors PM31, PM32 are connected to the power supply lines VDD. Gates of the pMOS transistors PM31, PM32 are connected to a drain of the pMOS transistor PM32. A drain (second node ND2) of the pMOS transistor PM31 is connected to the first node ND1. A drain of the nMOS transistor NM31 is connected to the drain of the pMOS transistor PM32, a gate thereof is connected to a constant voltage line VGS1, and a source thereof is connected to a ground line VSS.